

FIG. 1

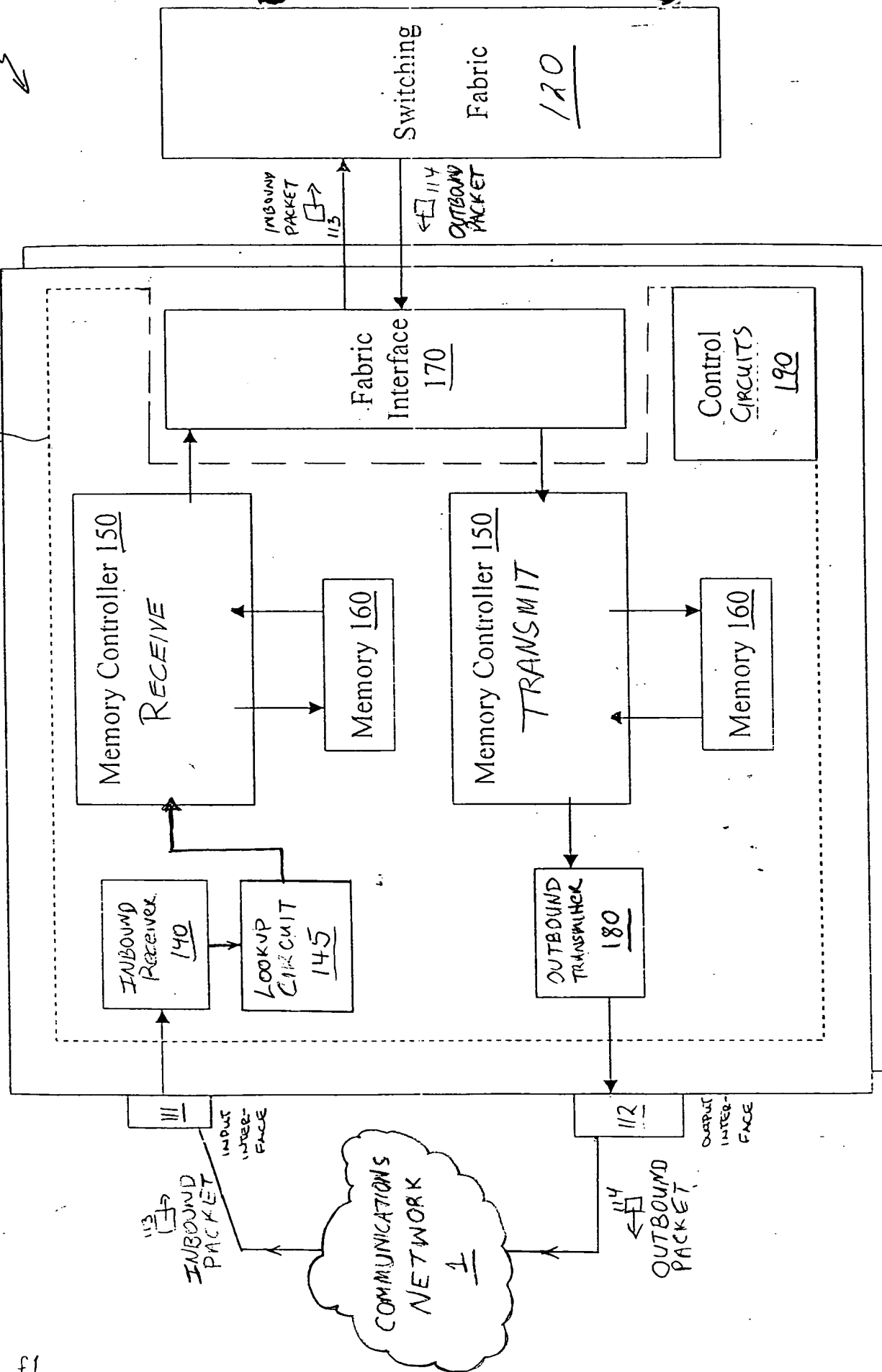
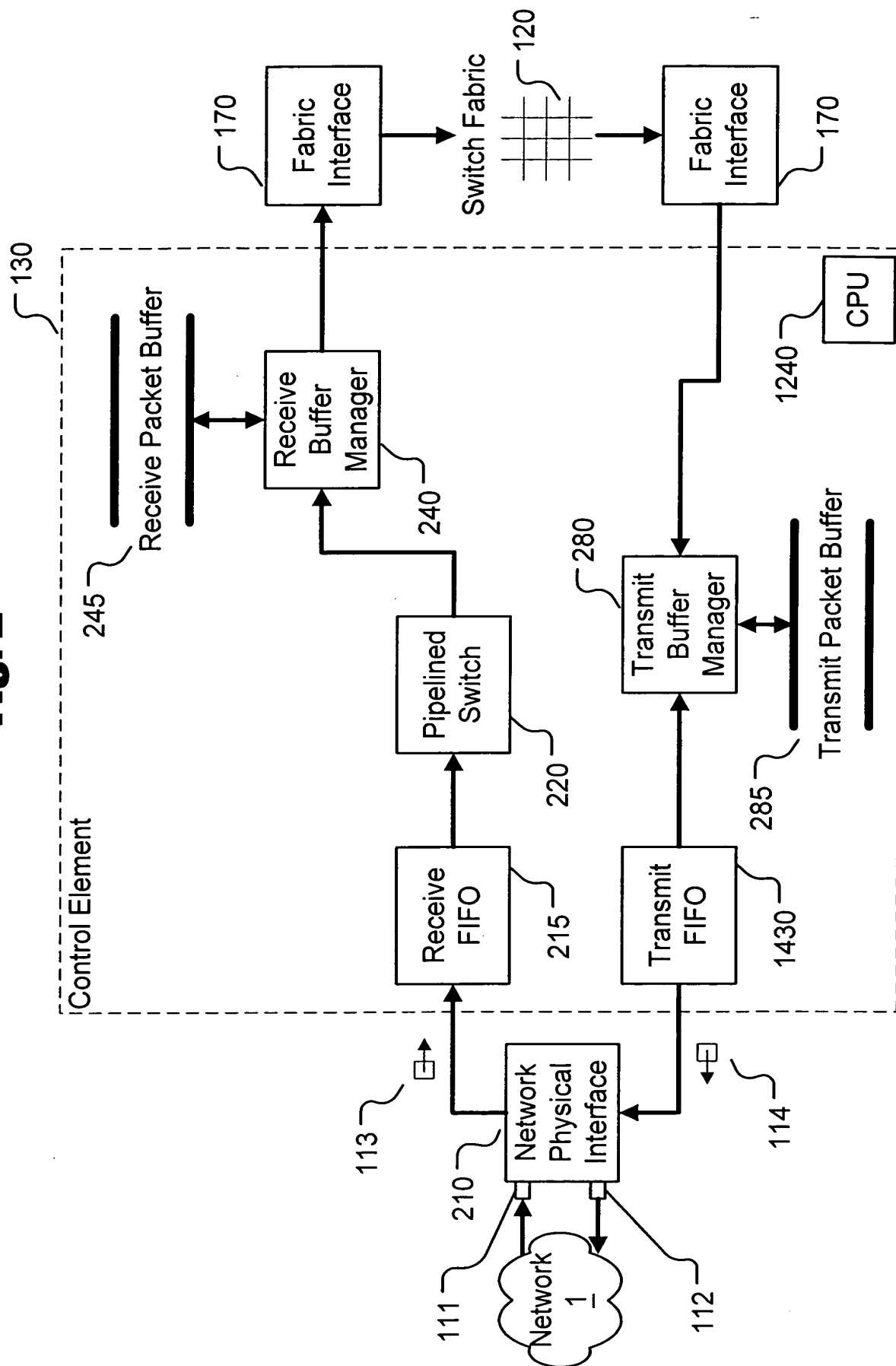
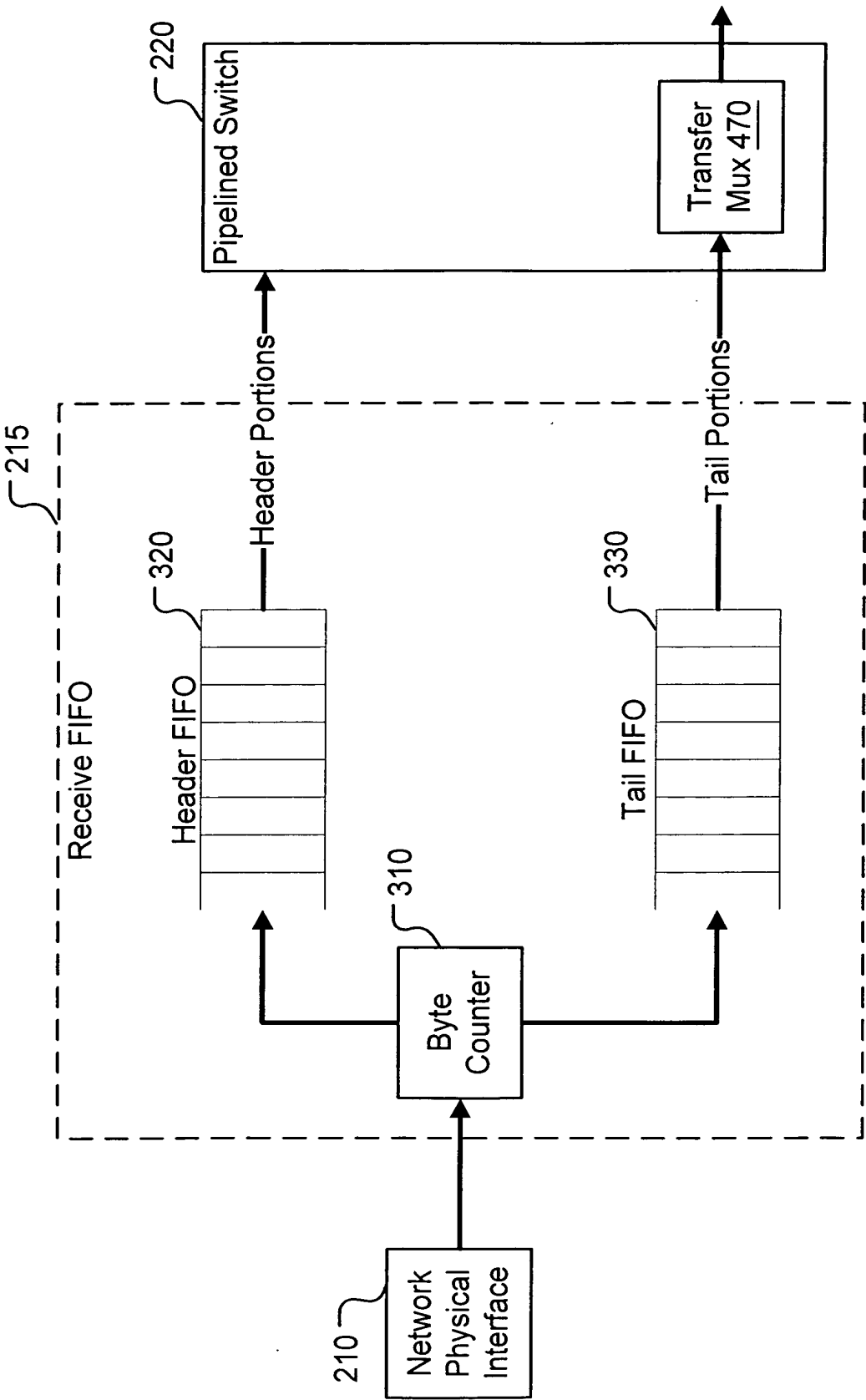


Fig. 2



+

Fig. 3



+

Fig. 4

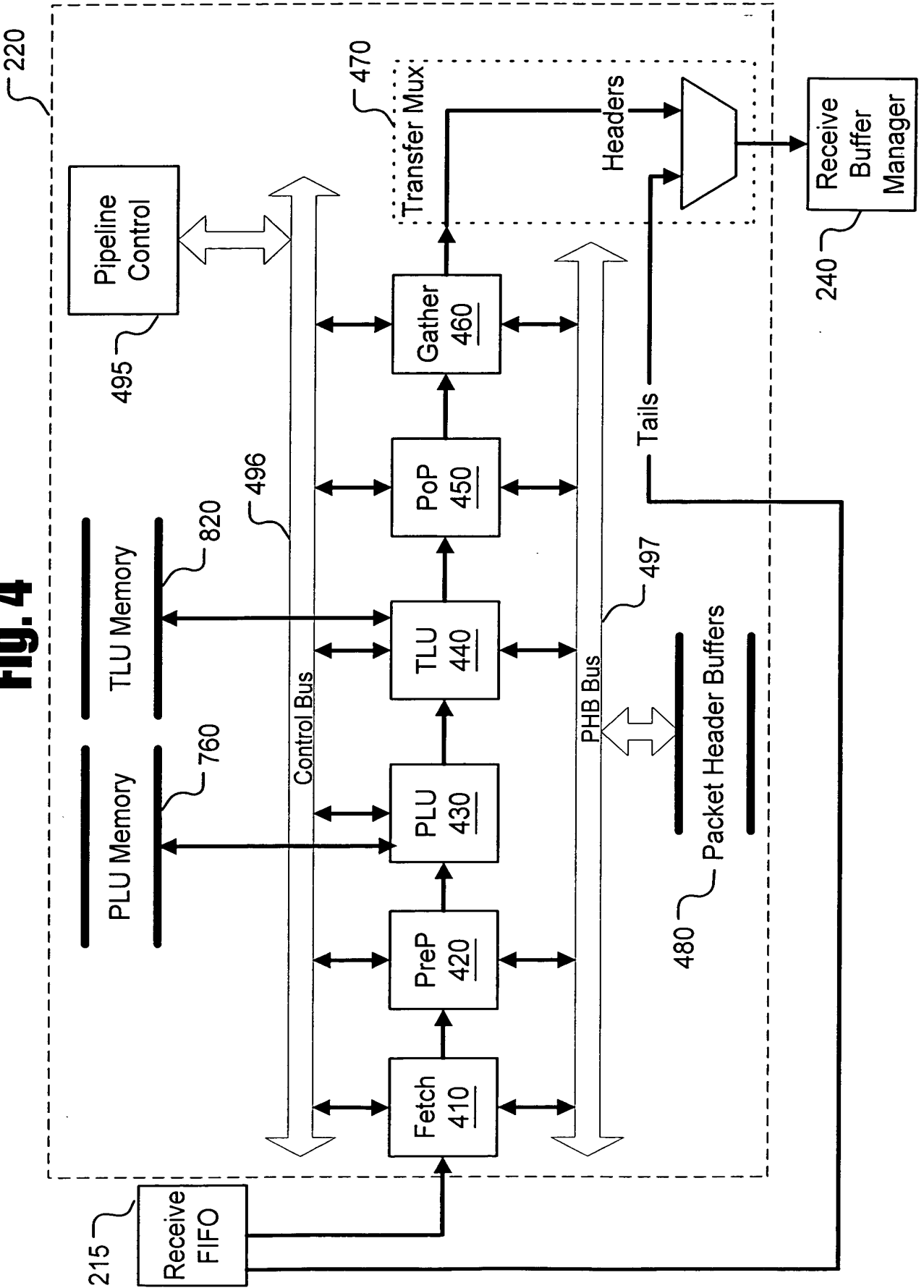


Fig. 5

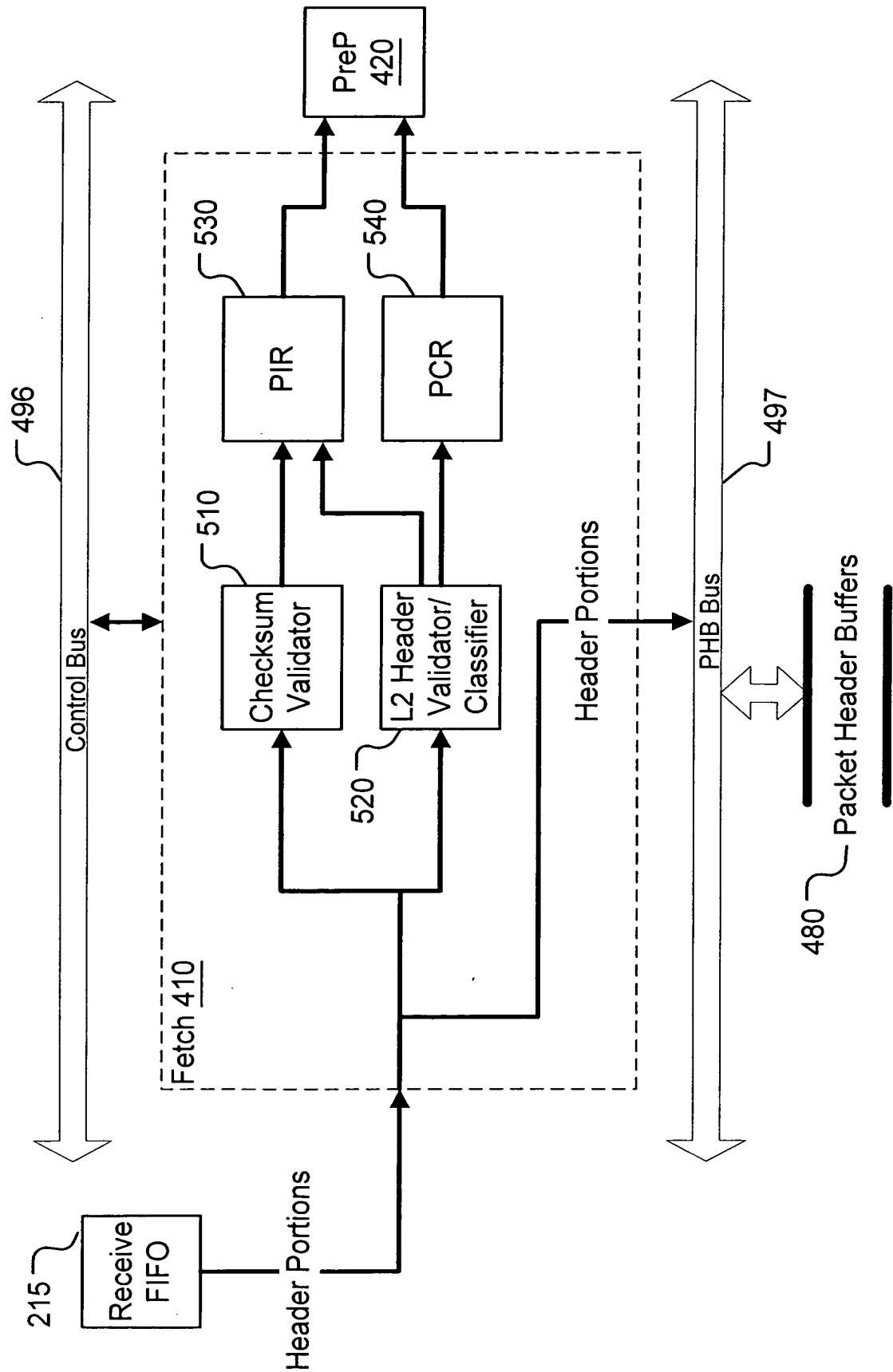


Fig. 6

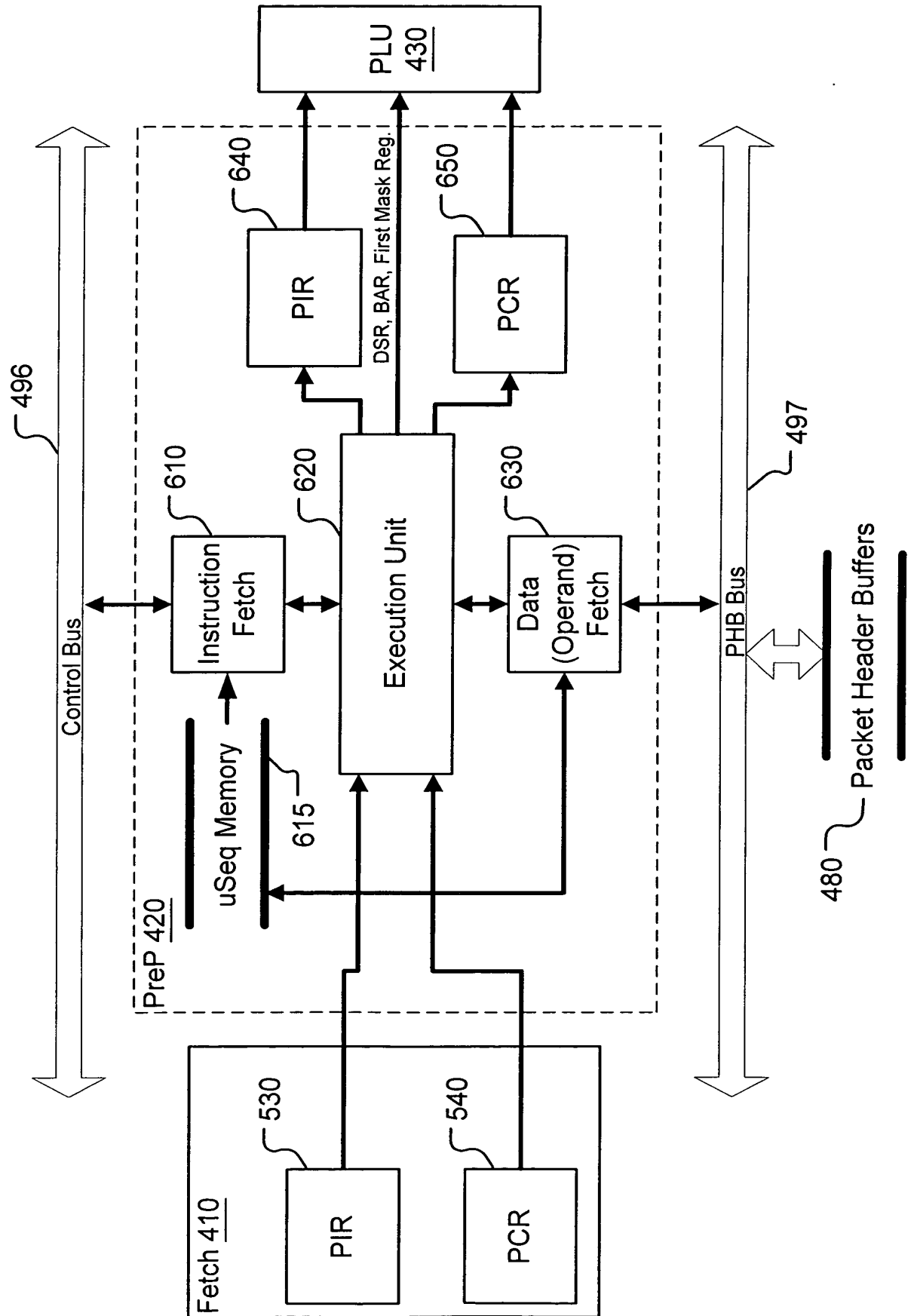
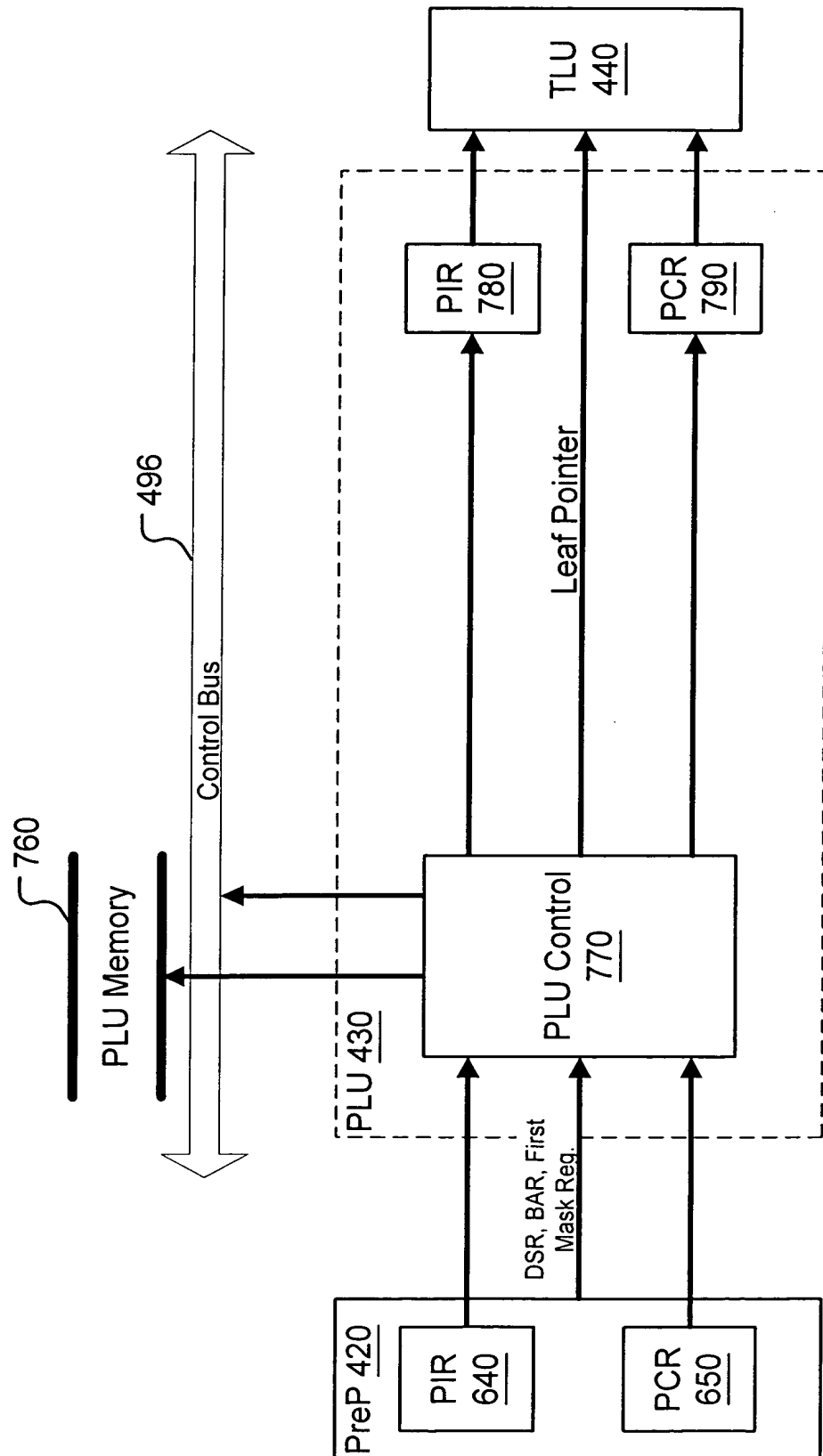


Fig. 7



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Fig. 8

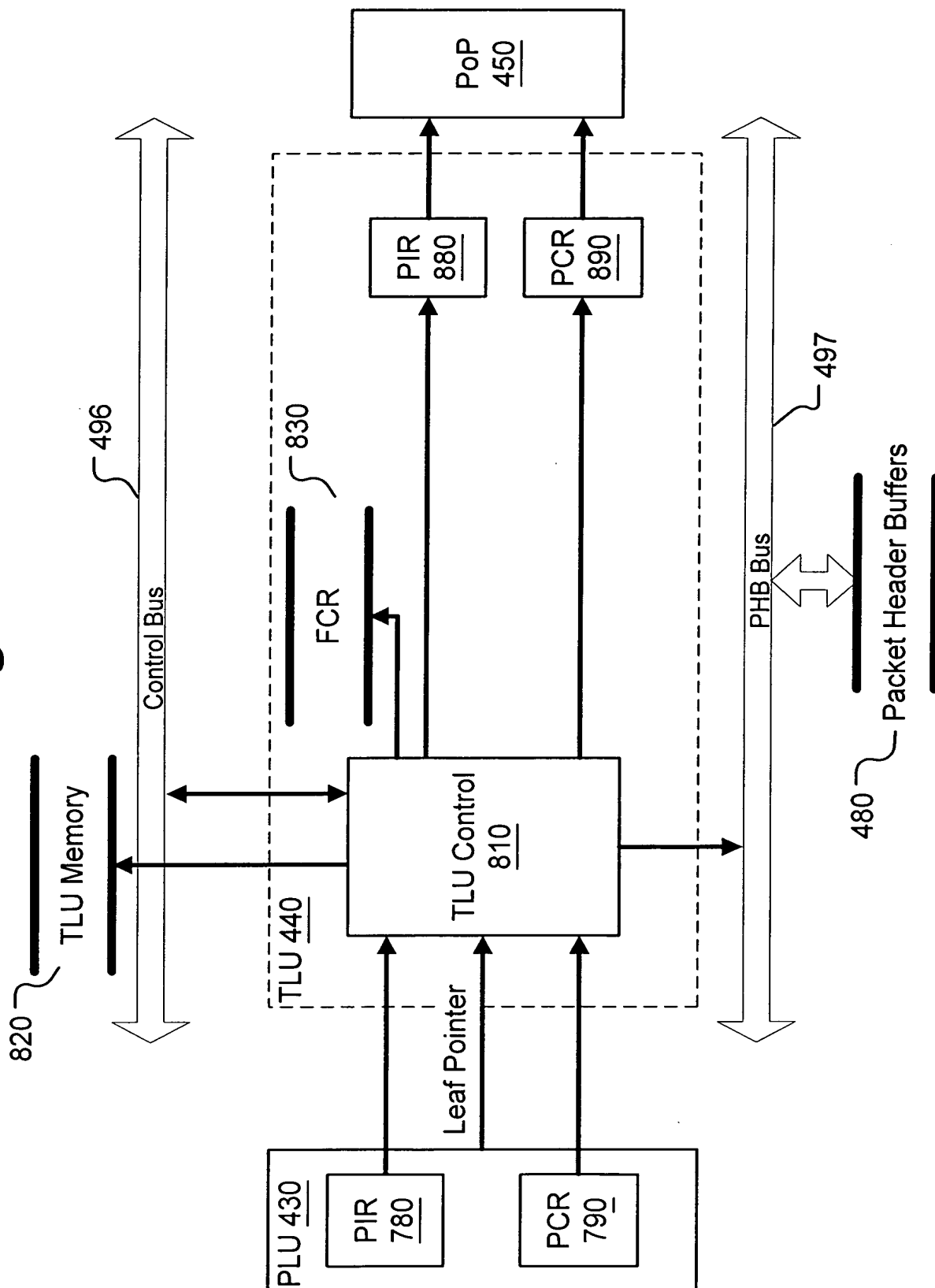


Fig. 9

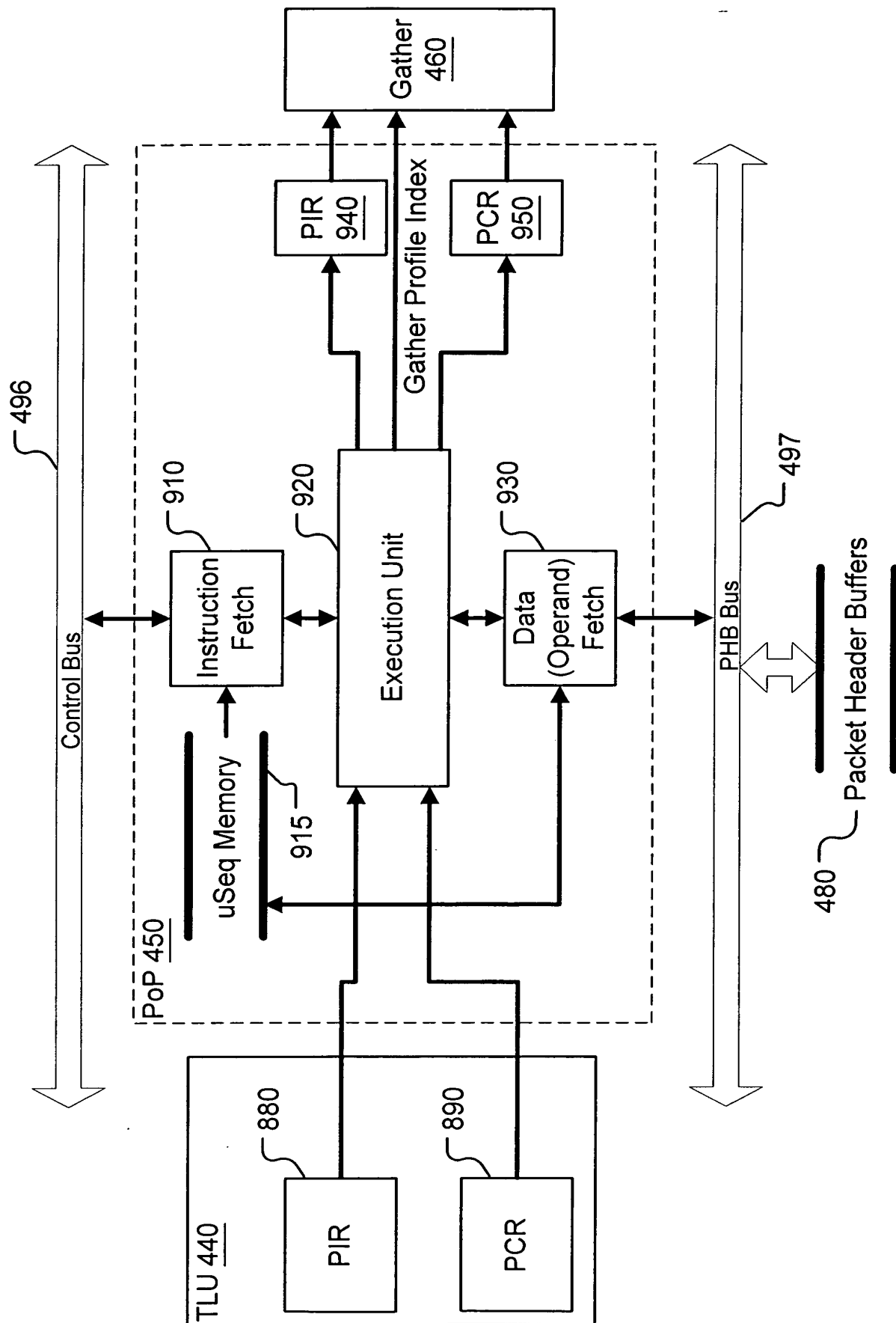


Fig. 10

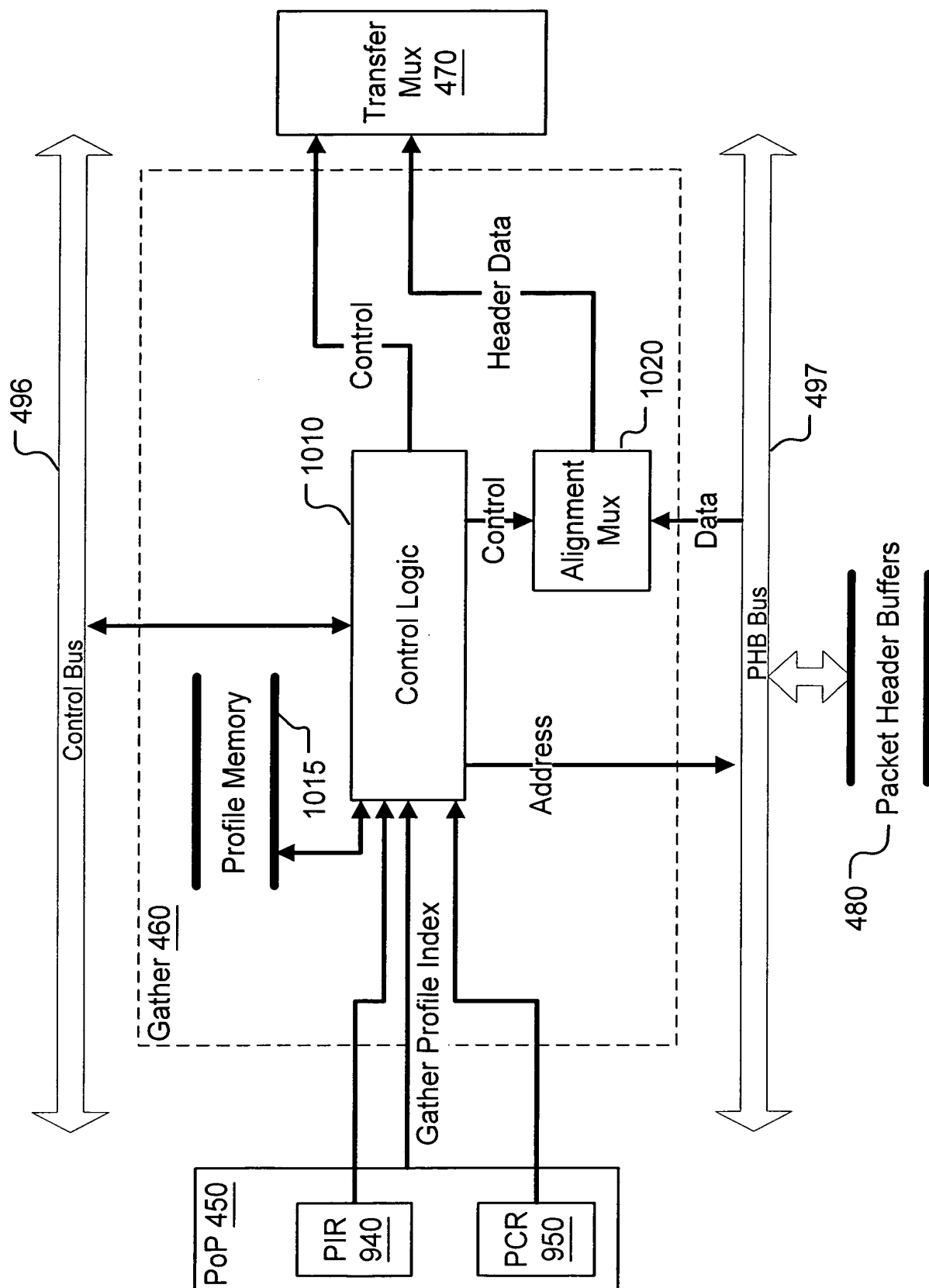


Fig. 11

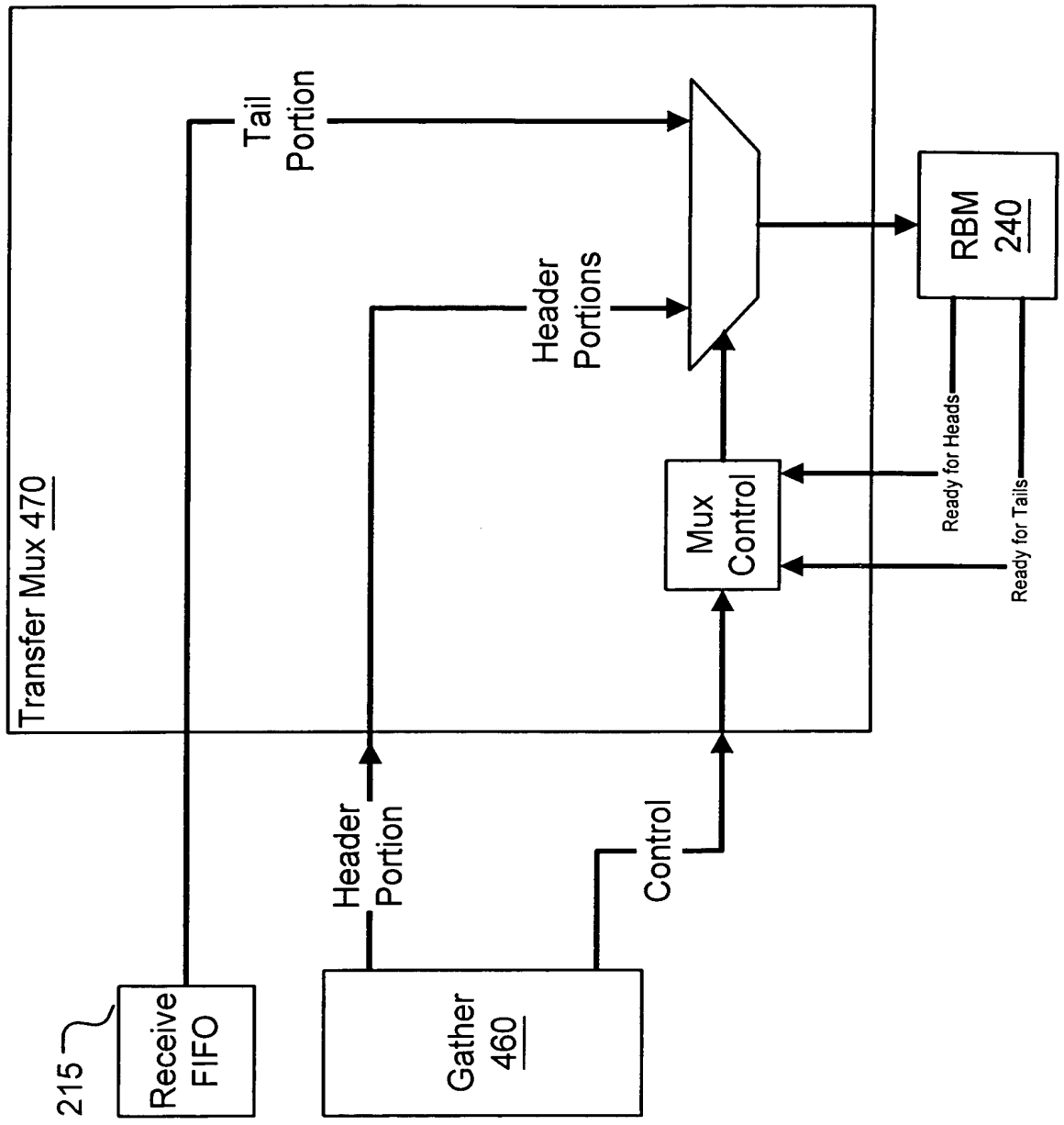


Fig. 12

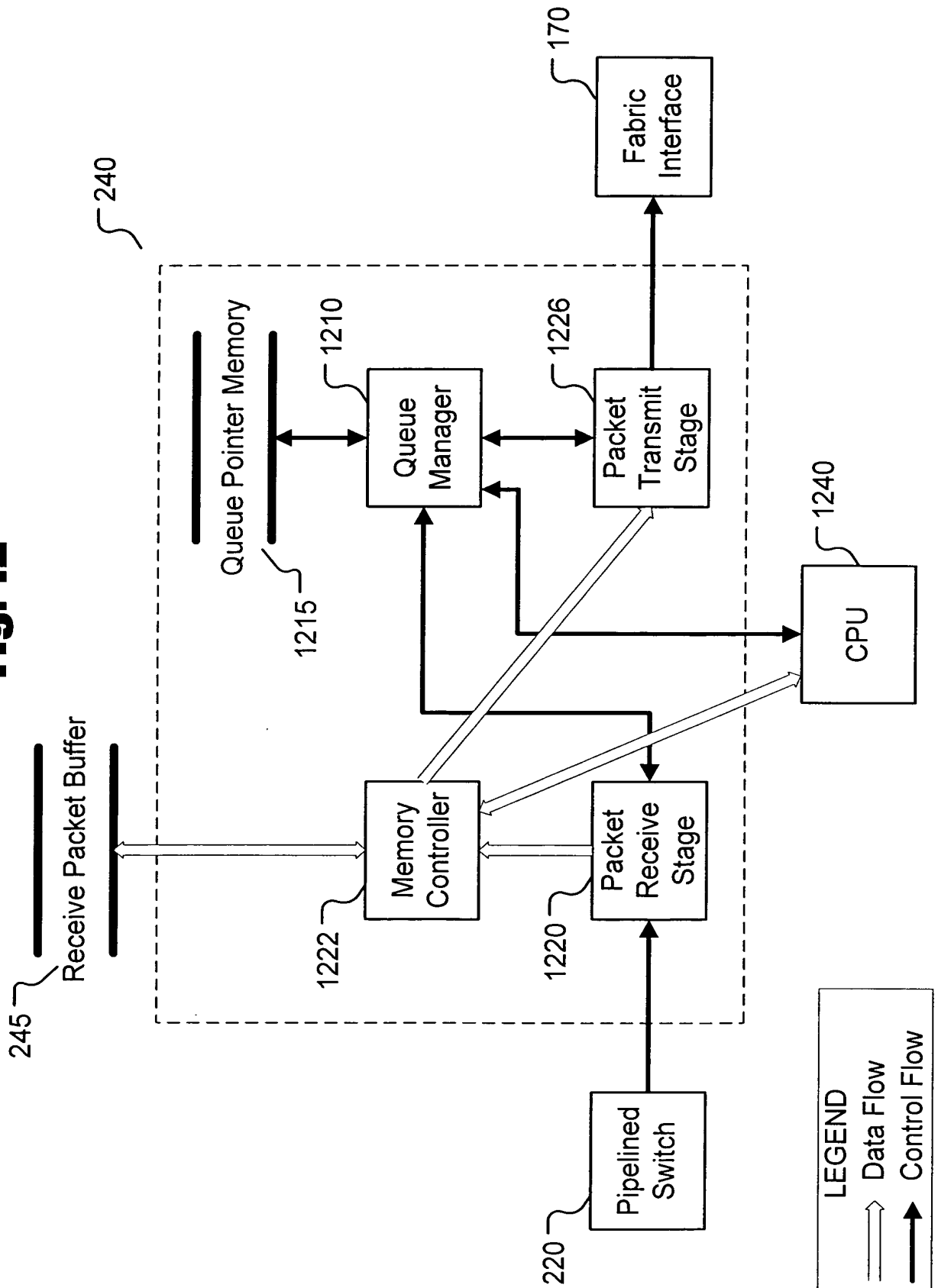
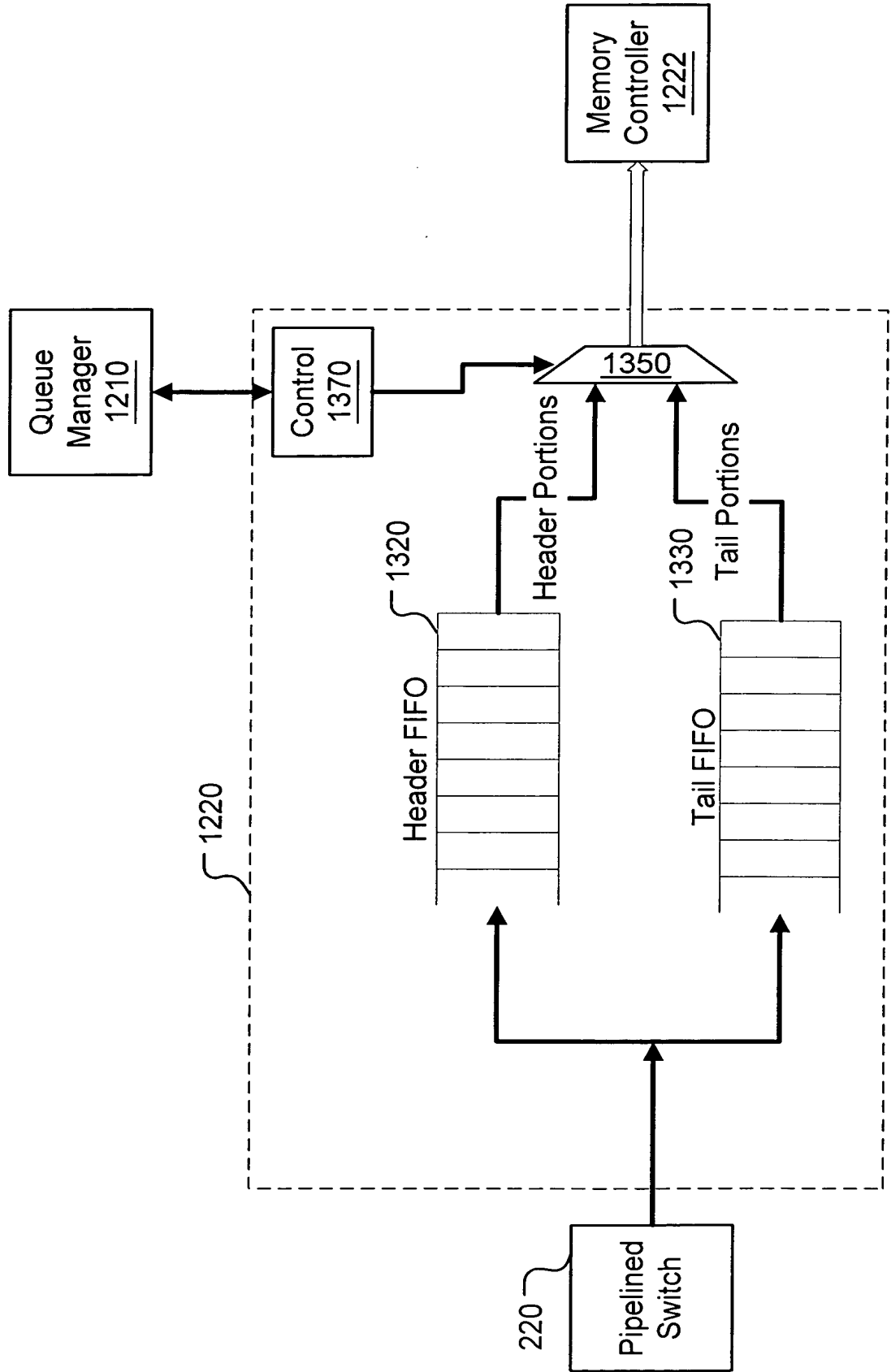




Fig. 13



Queue Pointer Memory 1215

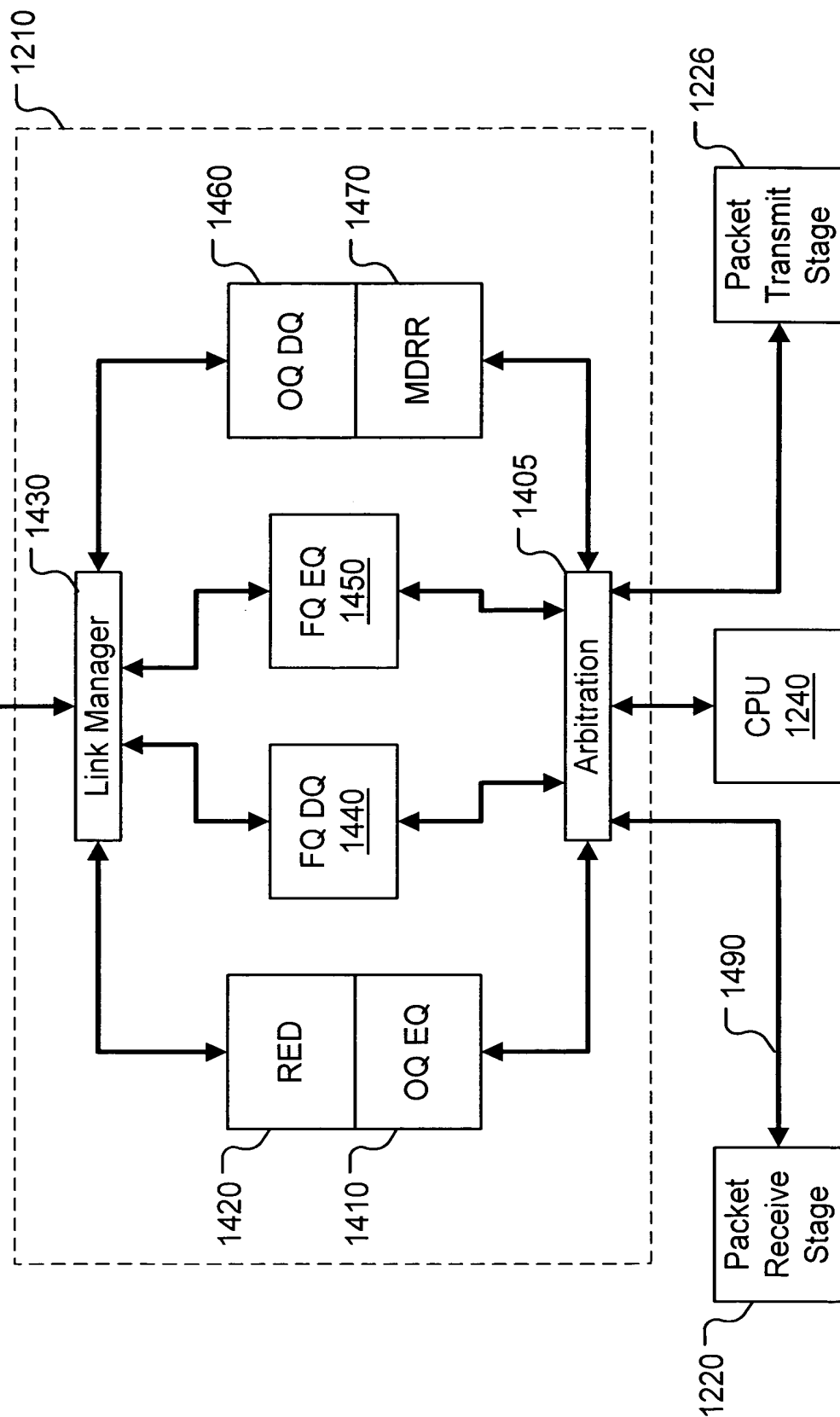
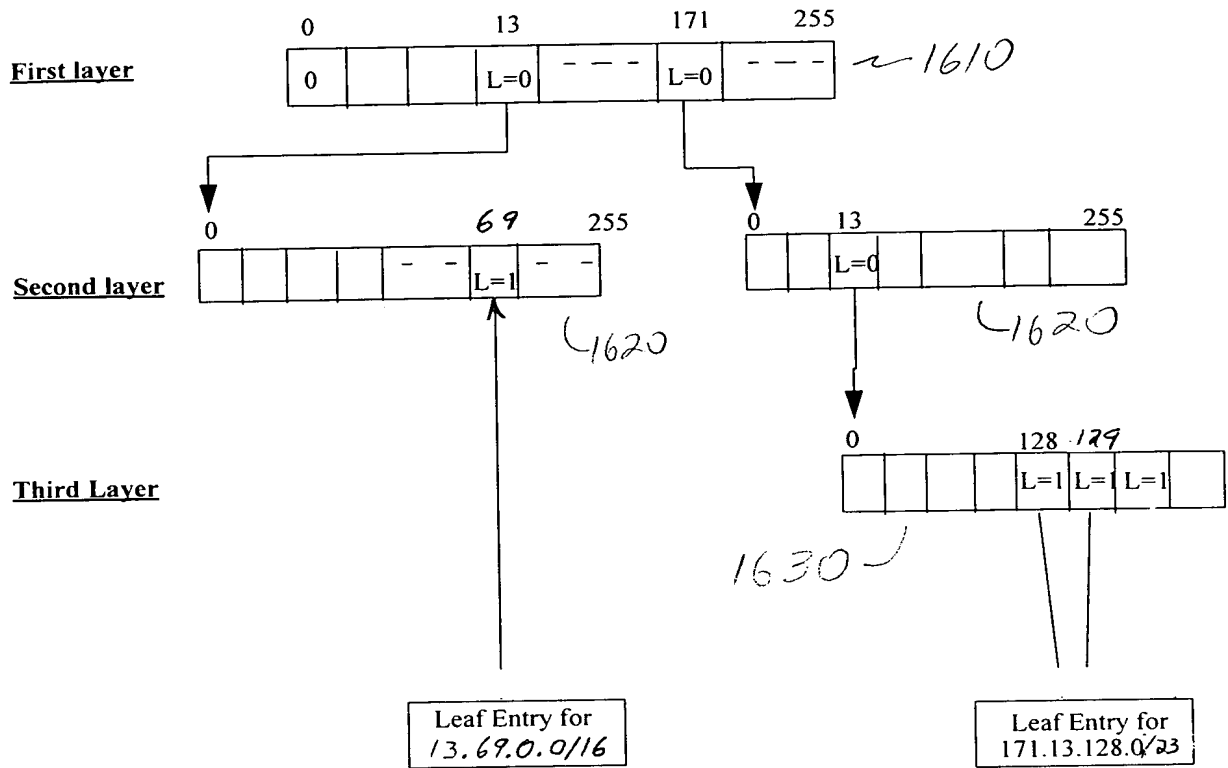




FIG. 16



00000000
FIG. 17

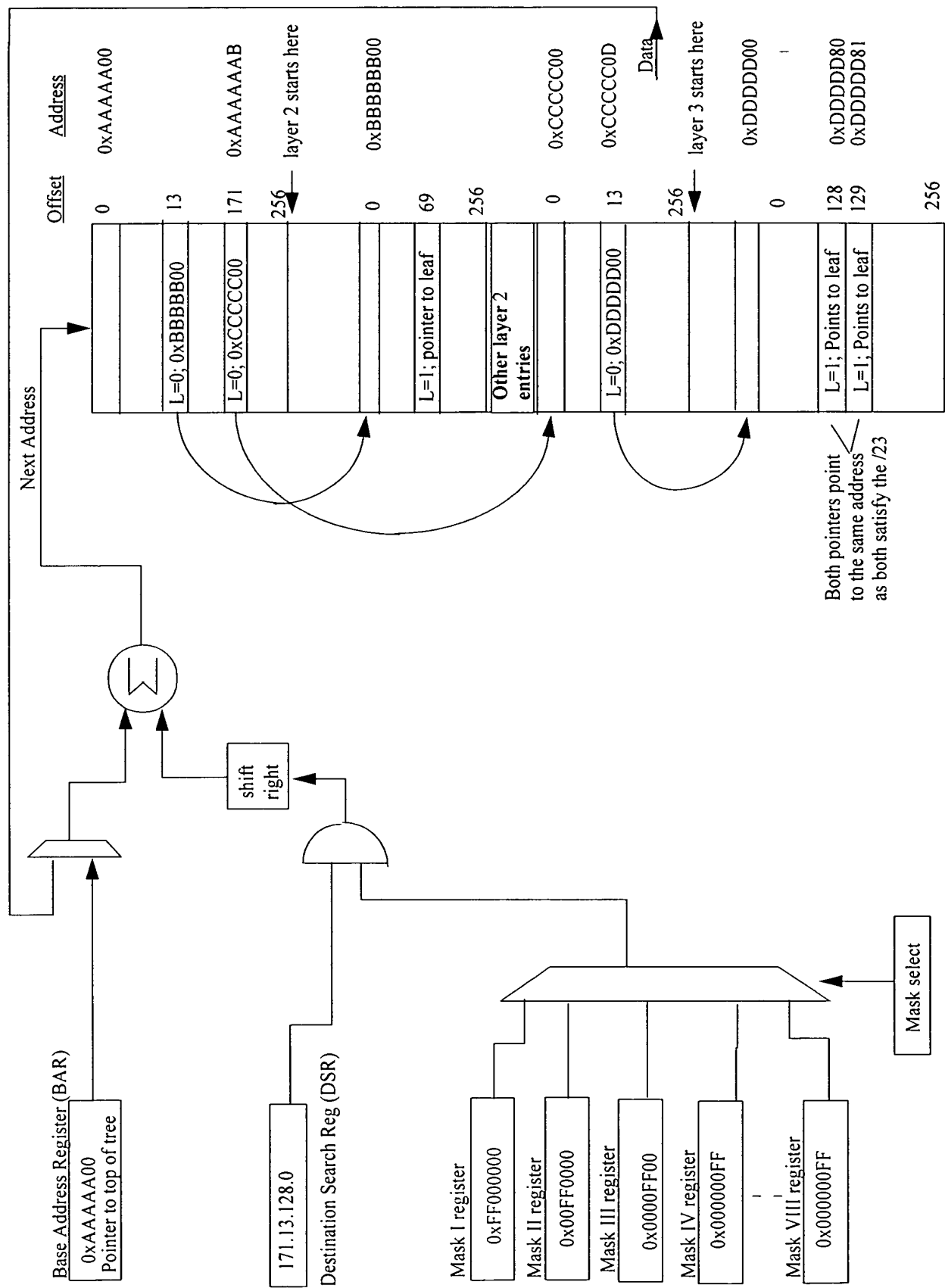


Figure 1 is a block diagram of the TLU logic. It shows a Base Address Register (BAR) containing the value 0xAAA000000 and a pointer to the top of the tree (labeled 1810). This points to a summation block (Σ). The other input to the summation block is the output of a shift right block. The shift right block takes input from a Mask select=VIII register and a Mask VIII register (0xFFFFF000). The output of the summation block is 0xAAA000004, which points to a TAG look up table in the PLU. The table has entries for L=1 and L=0, with a pointer to TLU memory indicated. The output of the table is data out.

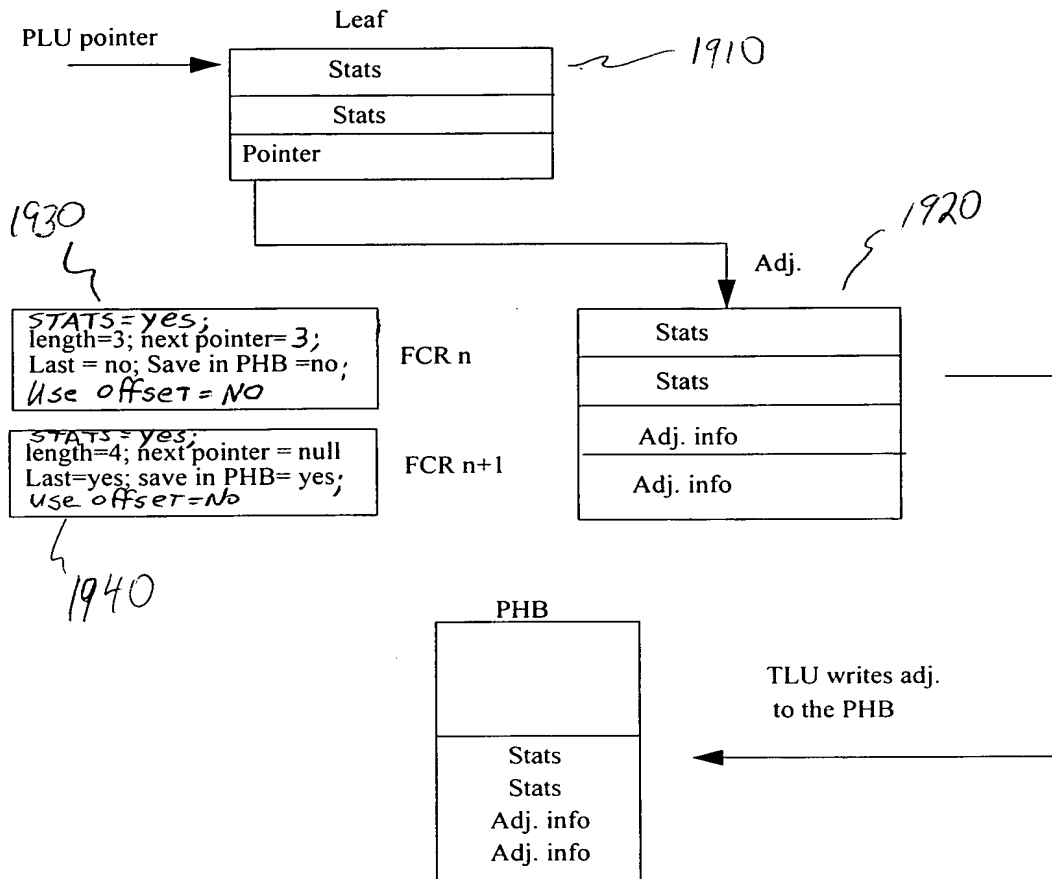
[illegible]

FIG. 20

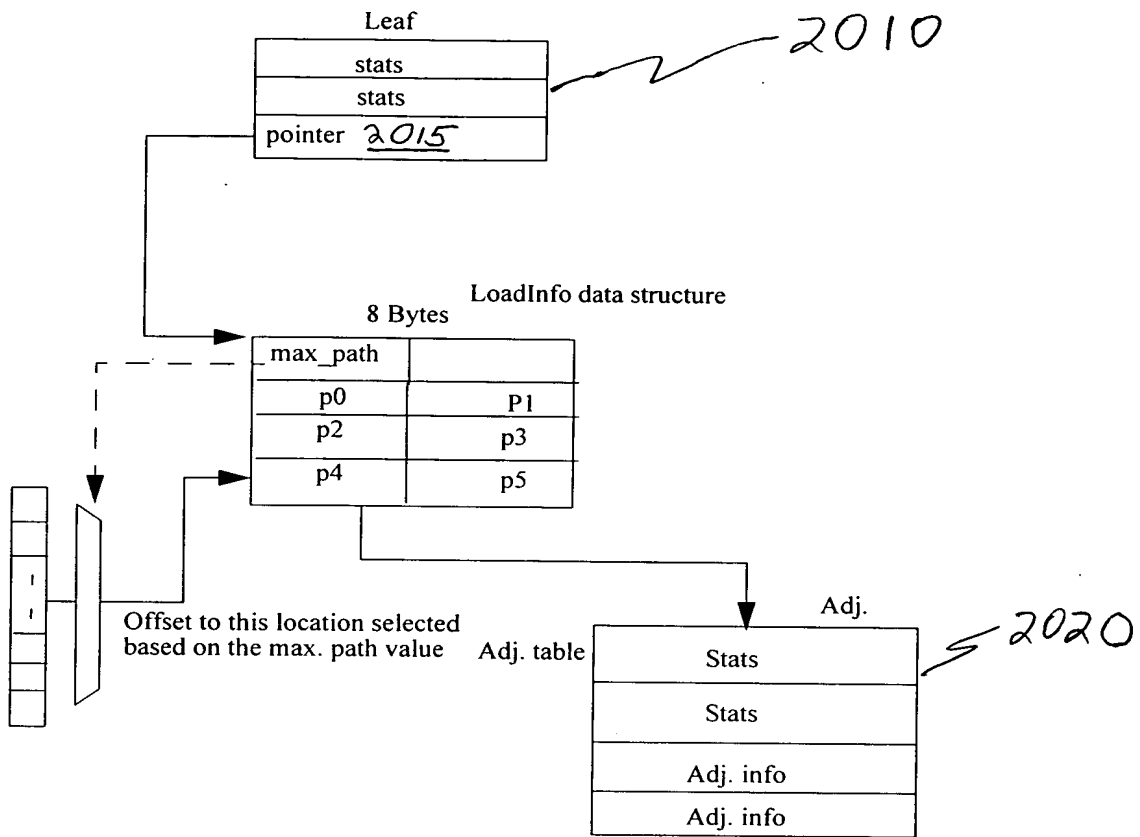


FIG. 21

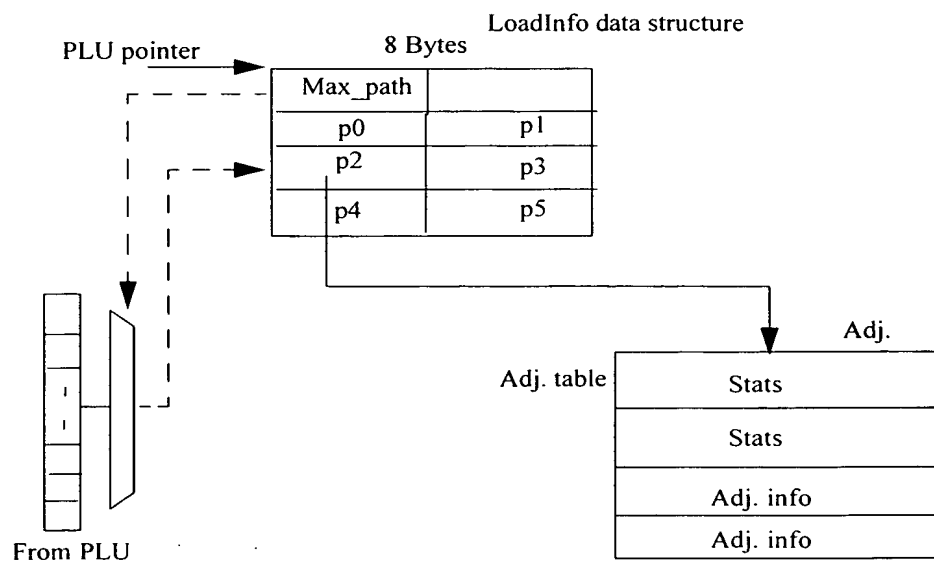


FIG. 22

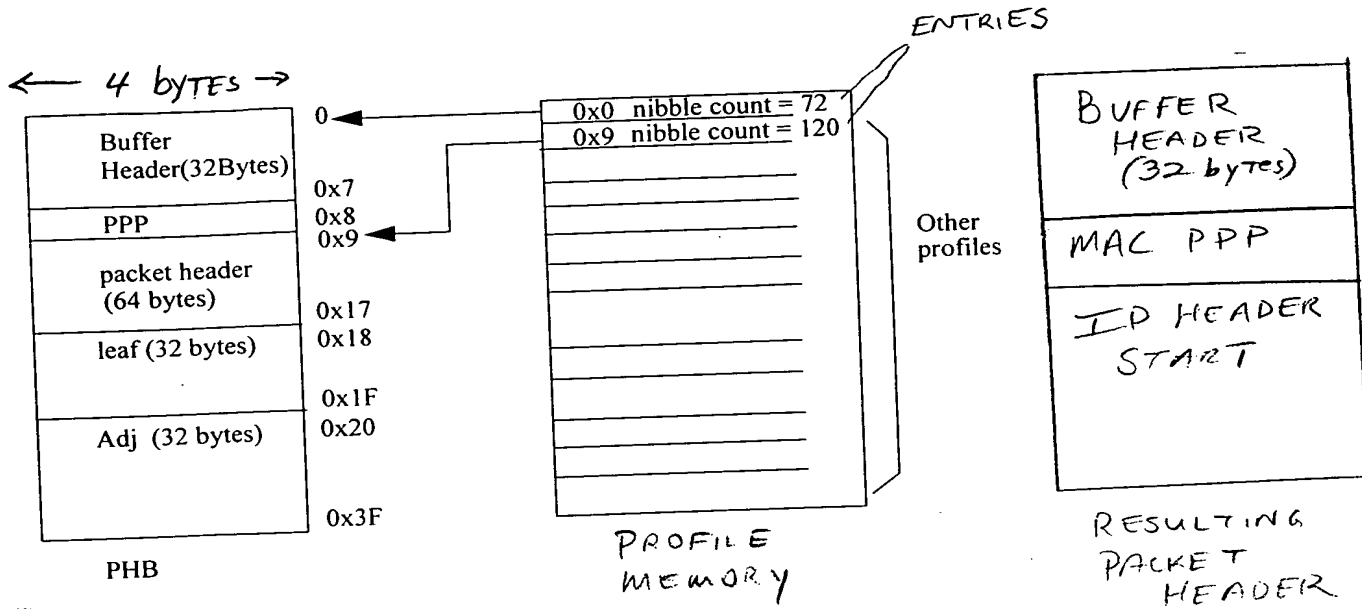


FIG. 23

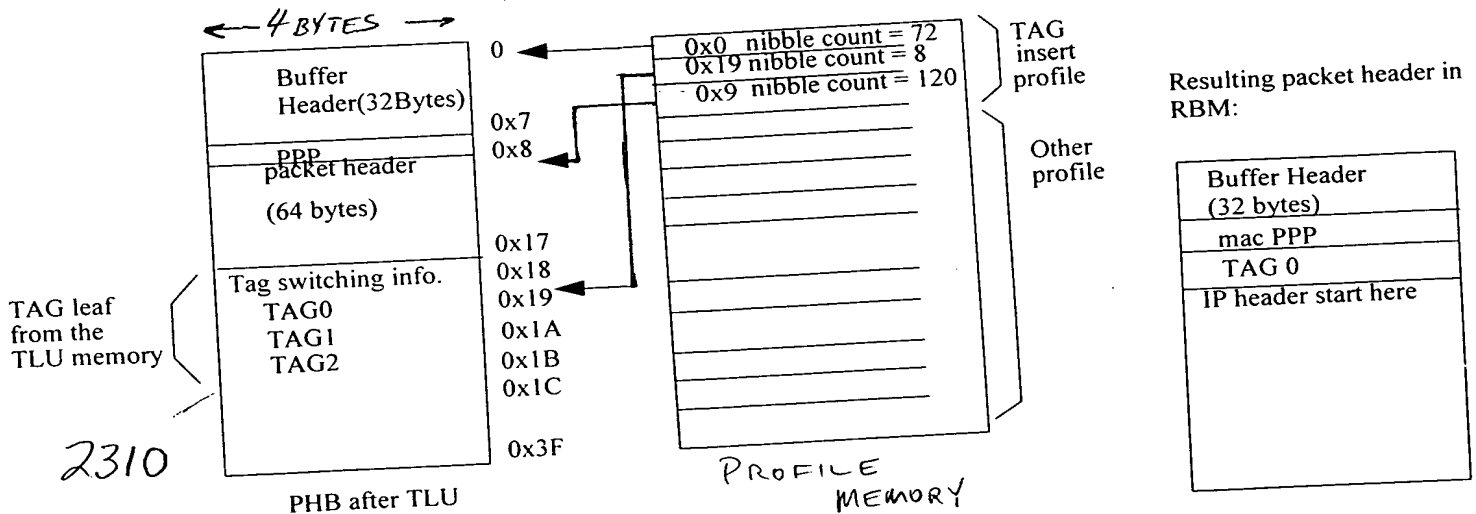


FIG. 24

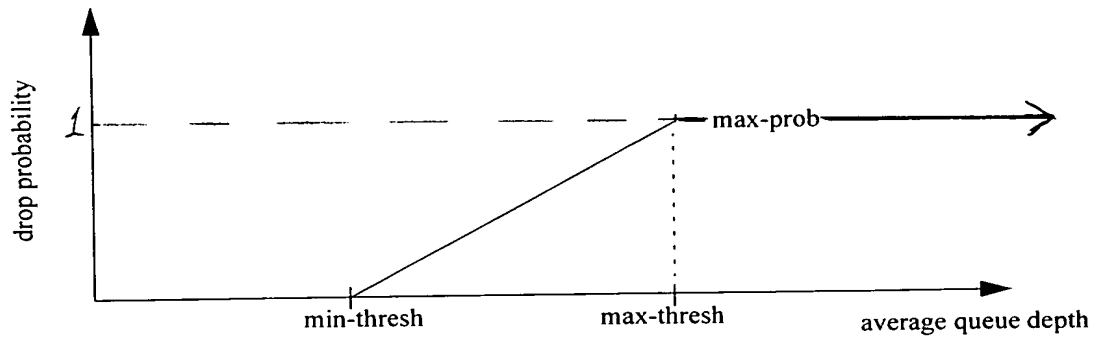


FIG. 25

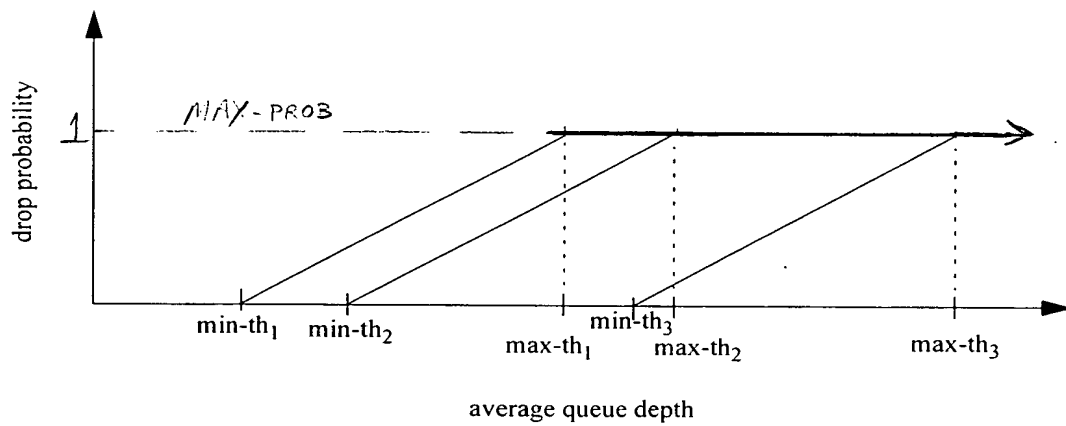
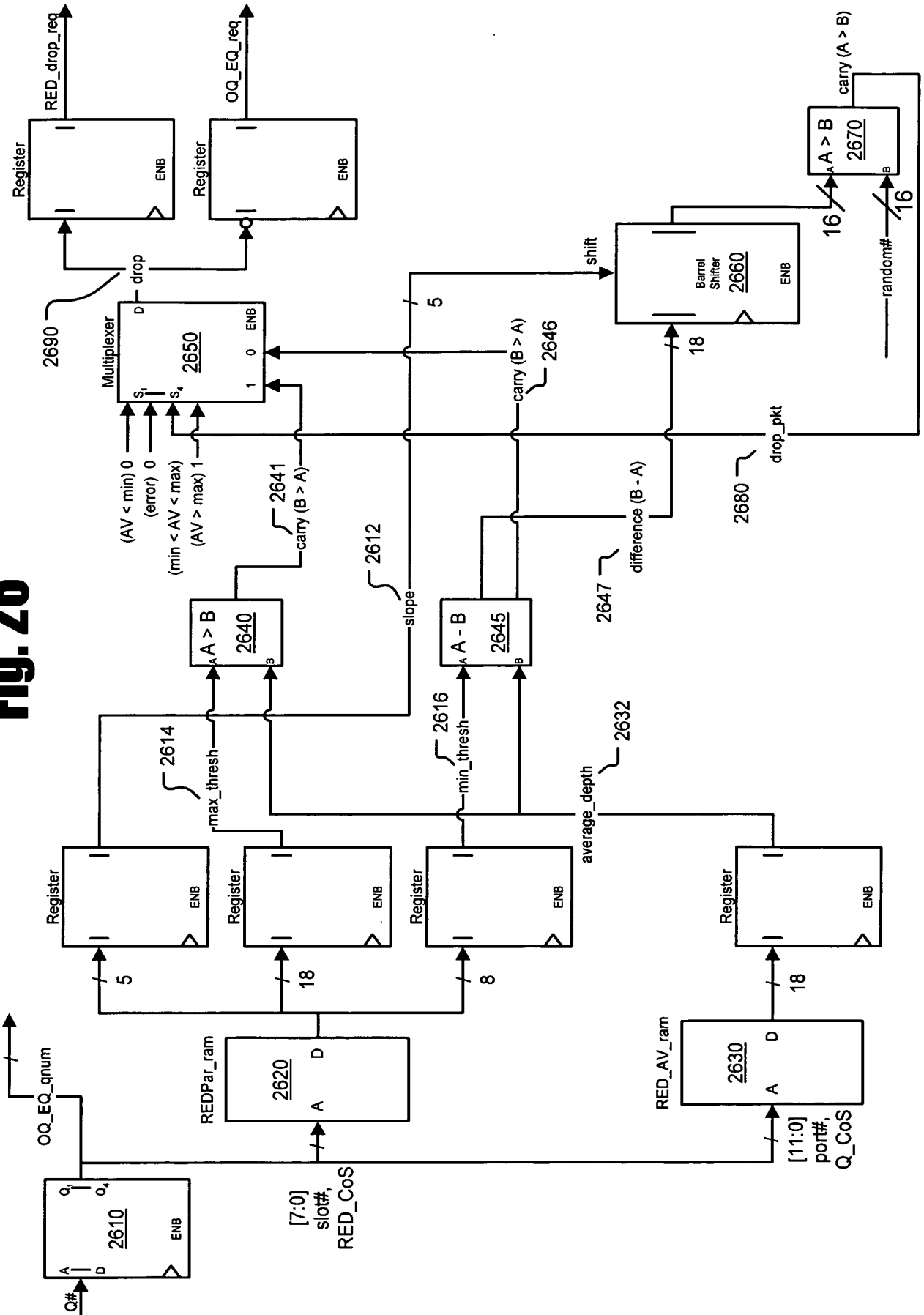
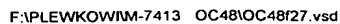


Fig. 26





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Fig. 28

2710

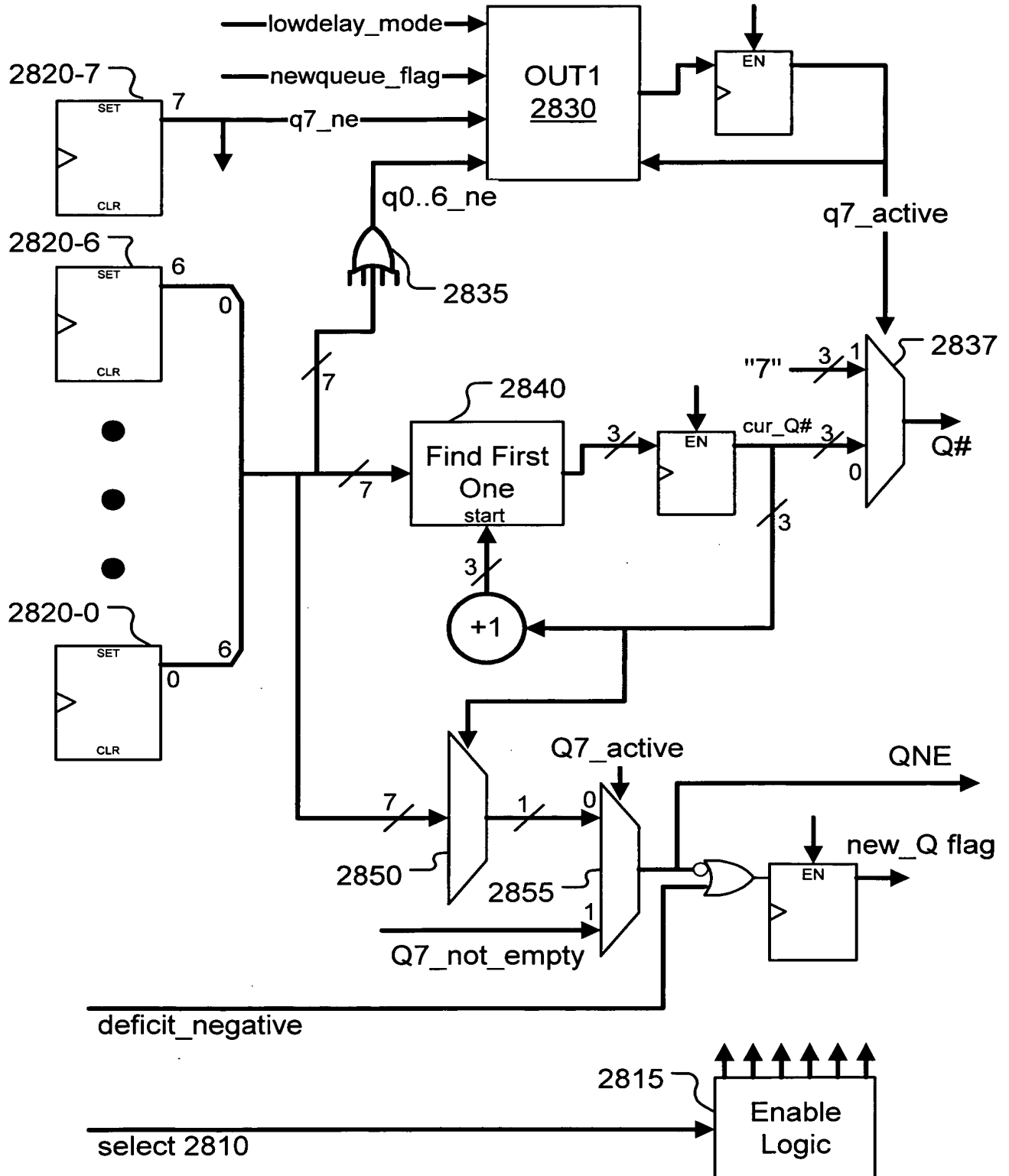
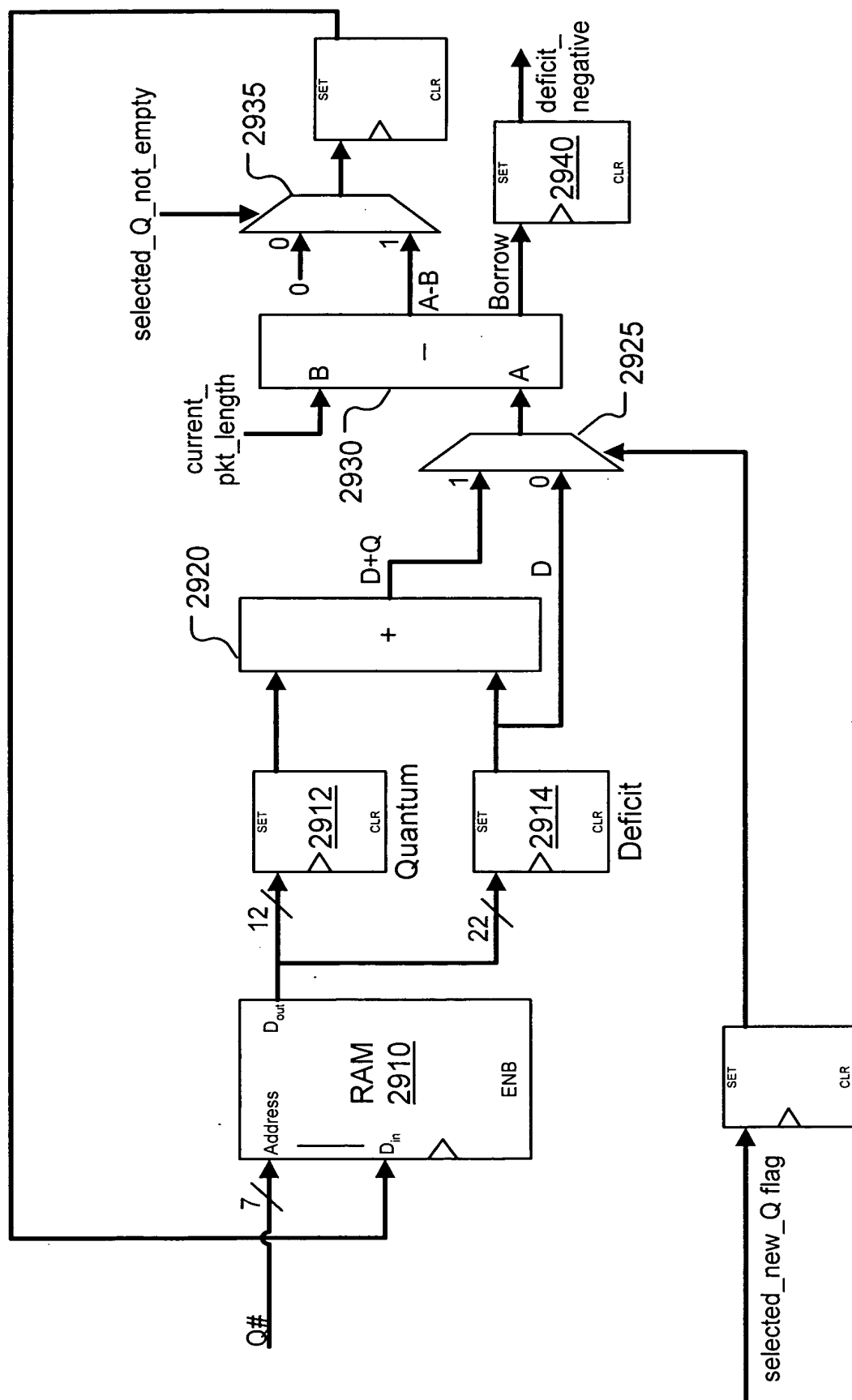


Fig. 29

2720



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FIG. 30

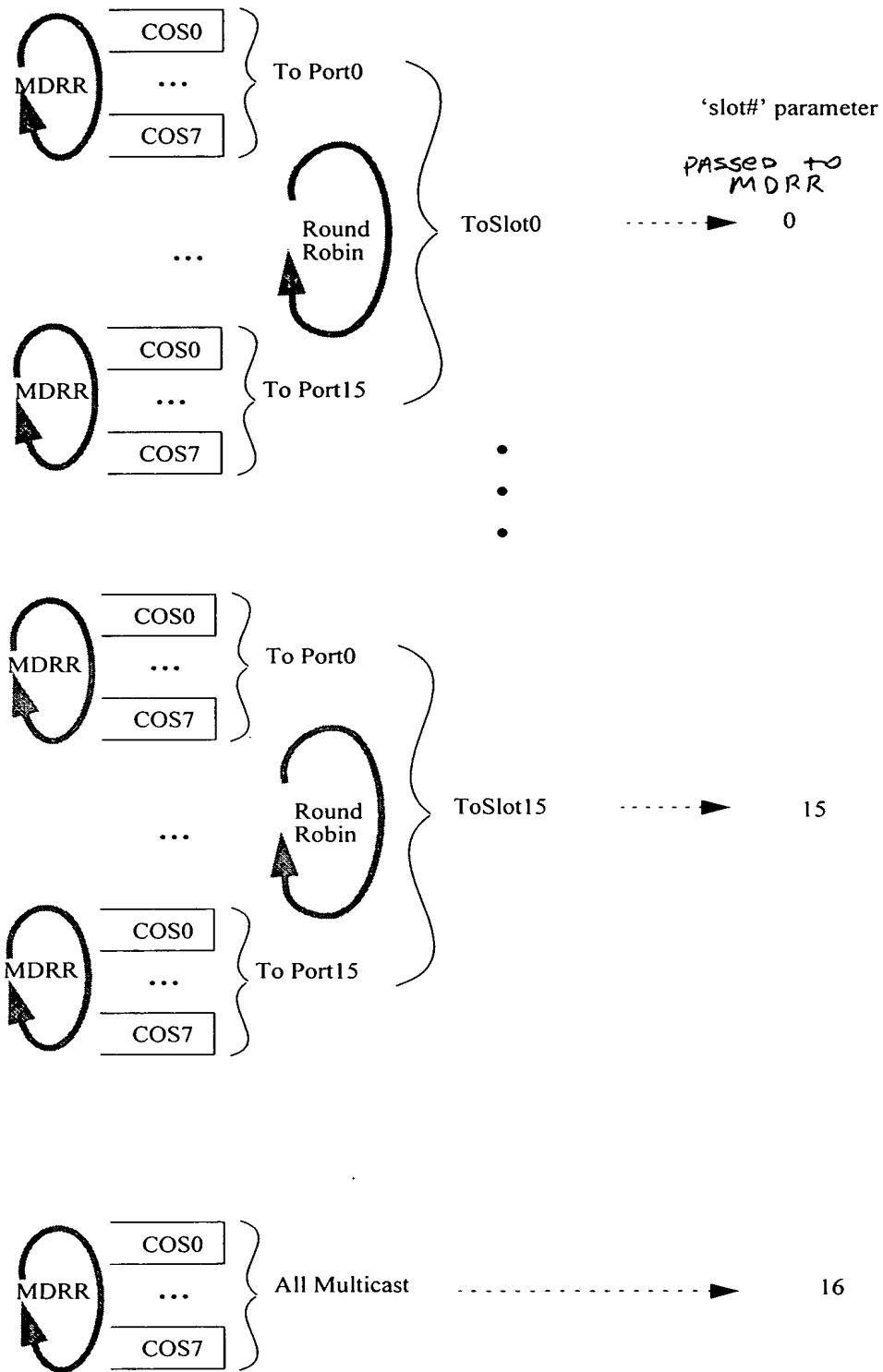


FIG. 31

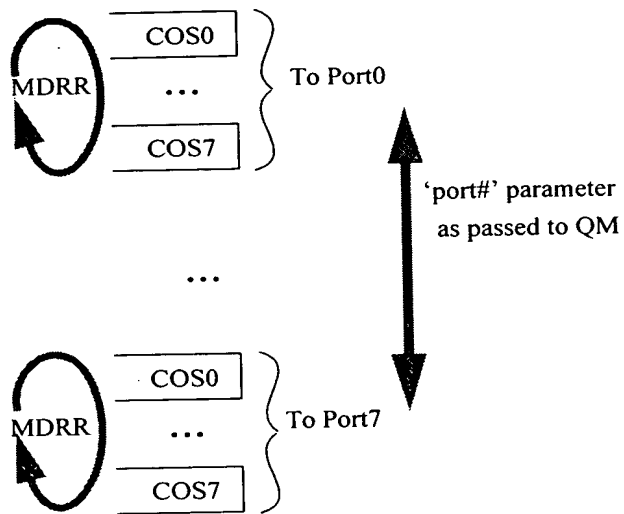


Fig. 32

